



# Real-Time Data Reorganizer for the D0 Central Fiber Tracker Trigger System at Fermilab

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**Abstract**--A custom digital data Mixer system has been designed to reorganize, in real time, the data produced by the Fermilab D0 Scintillating Fiber Detector. The data is used for the Level 1 and Level 2 trigger generation. The Mixer System receives the data from the front-end digitization electronics over 320 Low Voltage Differential Signaling (LVDS) links running at 371 MHz. The input data is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs). The data is then re-serialized at 371 MHz by LVDS transmitters over 320 LVDS output links and sent to the electronics responsible for Level 1 and Level 2 trigger decisions. The Mixer System processes 311 Gigabits per second of data with an input to output delay of 200 nanoseconds.

## I. INTRODUCTION

The D0 experiment [1] is sited at a high-energy particle accelerator, the Tevatron Collider, at the Fermi National Accelerator Laboratory (Fermilab) in Batavia, Illinois, USA. Fermilab is a High-Energy Physics research laboratory operated by Universities Research Association for the US Department of Energy. The D0 Detector is located in the Tevatron where protons and anti-protons traveling close to the speed of light in opposite directions collide. The purpose of the D0 detector [2] is to study these high-energy particle interactions. A component of the D0 Detector is the *Central Fiber Tracker (CFT)*. The CFT is constructed of scintillating fibers that are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders. The energy deposited into a scintillating fiber by particle interactions is transformed into visible light. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it, reaching a very sensitive light detector, the *Visible Light Photon Counter (VLPC)* [3], hosted in a liquid helium cryostat. The VLPCs are a derivative of solid-state photomultipliers and are used to convert the scintillation light into electrical signals. These are discriminated and digitized by the *Analog Front-End boards (AFEs)* [4]. The Mixer system receives the digitized data from the AFEs, then processes and re-organizes it in real-time with

minimal delay from cylindrical geometry into 80 azimuthal wedges or sectors. The restructured data are transmitted to the *Digital Front End board (DFE)* [5, 6] system. The DFE system uses the data to detect tracks that are used to contribute to level 1 and level 2 trigger decisions.

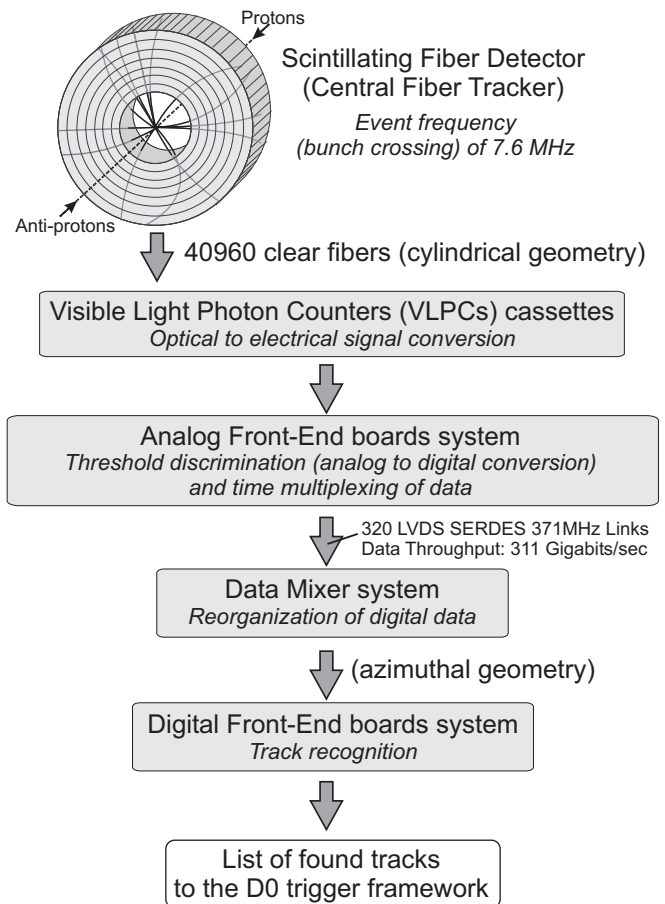


Fig. 1. Block diagram of the Central Fiber Tracker Electronics. Particles generated by proton anti-proton collisions deposit energy on the scintillating fibers where it is transformed into visible light. The light is carried by clear fibers to the Visible Light Photon Counters and converted to electrical signals. These signals are discriminated and digitized by the Analog Front-End boards, reorganized from cylindrical geometry into azimuthal sectors by the Data Mixer system and then used by the Digital Front-End board system for track recognition. Tracks are used for Level 1 and Level 2 trigger generation.

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The decision to design and build the Mixer system was made after all the other Central Fiber Tracker electronics system

components were almost in the production phase. The track recognition electronics (Digital Front-End board system) needed to receive the data organized in azimuthal wedges or "trigger sectors". Unexpected difficulties arose in physically reorganizing the optical fibers in trigger sectors before the front-end electronics performing the opto-electrical conversion and the digitization. The mechanical design of the detector did not allow for the fiber ribbons to be arranged as desired. The best option to solve the issue was the reorganization of the data after the digitizing process, which led to the design of the Real-Time Data Reorganizer or Data Mixer System [7].

## II. DESIGN REQUIREMENTS

Because the Mixer System was specified as a late addition to a previously designed system, many design constraints were imposed. The most challenging constraints were the limited space available, the restricted access location, the system timing requiring minimal input to output delay, the number of input/output links, the clock/frame resynchronization of the input links data streams. A particular demanding constraint was the already fixed throughput of the Mixer System I/O links, just barely sufficient for the detector's data throughput. Due to limited budget and time available for the project, the specification also called for a custom design with minimal flexibility. Furthermore, the possible flavors of the Mixer board had to be based on the same hardware, so that only one board design would be needed. The fact that the system was to be installed in a limited access area also required the capability to remotely run diagnostics and remotely update the system firmware.

## III. DATA REORGANIZATION

A graphical software tool was designed and written to both find a conceptual solution for reorganizing and transferring data in compliance with the design specification and to implement that solution. The tool is based on the Microsoft Excel™ [8] software package and makes extensive use of routines written in Visual Basic™ for Applications (VBA). The tool allows graphical visualization and analysis of the data and its attributes. This capability was used to study the data flow and reorganization. The tool allowed the data to be arranged in order to both minimize the required number of interconnections between inner elements of the Mixer System and to reorganize the data into azimuthal trigger sectors. The tool was also used to compare possible hardware architectures, and after the architecture was chosen, to generate the portion of VHDL (Very high speed integrated circuit Hardware Description Language) code defining how the system's FPGAs should operate on the data [9]. This portion of the VHDL code is unique to each FPGA. Due to the large number of data bits (40960 at 7.6MHz) to be multiplexed, this code is also the most prone to error, in particular if the code it is manually typed. Our automated tool addressed these concerns.

## IV. DESIGN SOLUTION

The Mixer System consists of a 21-slot 6U subrack with a custom backplane [10]. The subrack type was constrained by the limited rack space available for new component in the Central Fiber Tracker electronics. The first Mixer subrack slot hosts a custom controller [6], and the remaining slots host twenty Mixer boards. These twenty Mixer boards can be logically partitioned into five subsystems of four boards each. This partitioning matches the fiber detector partitioning in five 72° wide sections referred to as supersectors. This mechanical symmetry allows each supersector to be considered identical and independent from the Mixer System's point of view. Each Mixer subsystem exclusively handles the data from one supersector. Due to the detector symmetry, all five Mixer subsystems can use the same firmware.

A portion of the data received by each of the Mixer boards, needs to be routed to another board in order to be part of the output data stream to where it belongs. This is accomplished using point-to-point connections on the custom subrack backplane. The input links to the Mixer System have been arranged in such a way as to limit each Mixer board's data exchange to only the two adjacent boards. Furthermore, the five Mixer subsystems can be considered independent, because no data exchange is needed between them.

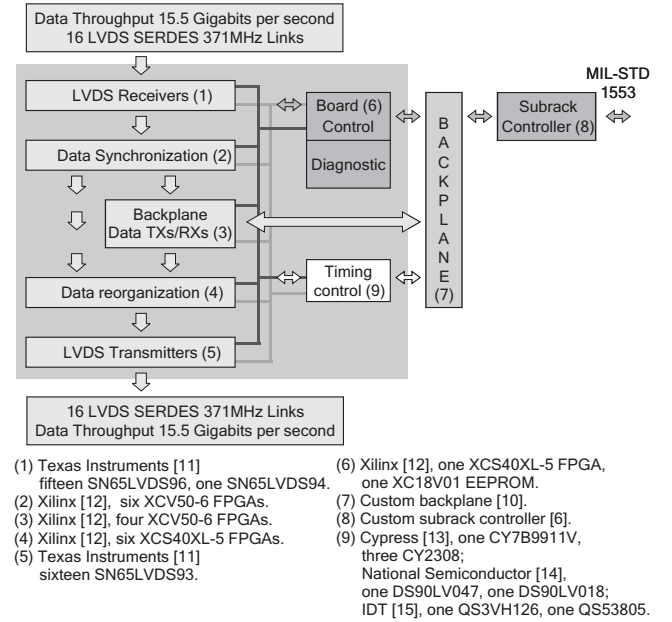


Fig. 2. Block diagram of a Mixer board showing data flow, controls, timing and external communication. A single Xilinx FPGA controls diagnostic and communication with the subrack controller. Timing logic is used to synchronize clocks and frames across an entire Mixer subsystem.

The Mixer System receives the data from the AFE boards over 320 LVDS serializer-deserializer (SERDES) [11] links running at 371 MHz. The input links are of two types. 300 are 21 bits wide serialized into four differential pairs and 20 are 28 bits wide serialized into three differential pairs. The input data

is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in FPGAs, and then re-serialized at 371 MHz by the LVDS transmitters. The system has 320 LVDS SERDES output links, all are running at 371 MHz and all are 28 bits wide. Of the 320 output links only 240 carry unique data. The remaining 80 links have replicated data, and are needed to transmit some of the data to more than one DFE system's module. The Mixer System processes 311 Gigabits of data per second, with an input to output delay of 200 nanoseconds. Of this, 48 nanoseconds are used for data de-serialization/serialization, and 152 nanoseconds are used for data re-synchronization and mixing.

## V. EMBEDDED DIAGNOSTICS

Embedded diagnostic firmware proved to be a critical component of the Mixer system [16]. It allows monitoring the correct status of several critical parameters of the input links: clock frequency, frame markers, control bits, clock synchronization, frame synchronization, and detection of test patterns. The diagnostic also provides for monitoring of the board local bus, the backplane serial and parallel buses, the FPGAs configuration status, the transmission of test patterns on the output links and testing the front panel LEDs.

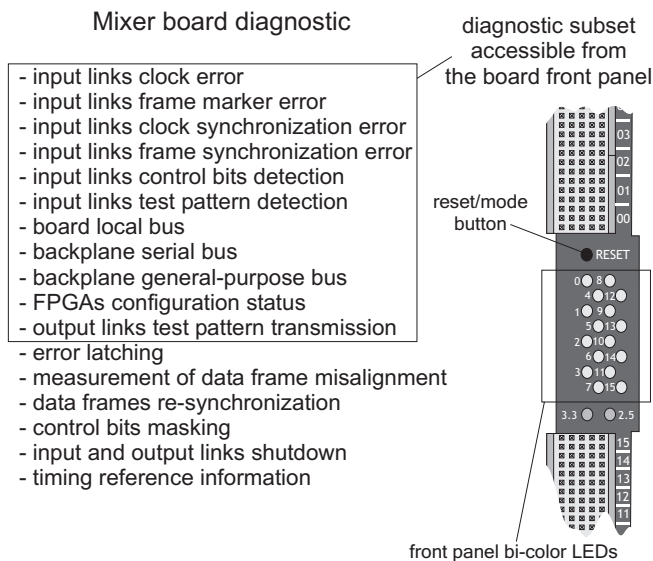


Fig. 3 Mixer Board diagnostic. The diagnostic is accessible through the subrack controller interface. A subset of the diagnostic information is accessible from the mixer board front panel. A dual function push-button allows the user to reset the board and also to select one of the 16 sets of signals to be displayed via the front panel LEDs.

The input links test pattern recognition and output links test pattern transmission is used by the Central Fiber Tracker electronics diagnostic to verify the integrity and correctness of the cabling. The Mixer diagnostic is remotely accessible through the MIL-STD-1553 system interface.

A simplified version of the diagnostic uses the reset/mode push-button and 16 bi-color LEDs on the Mixer board front panel. This allows the user to view, in real-time, the status of 256 signals and flags by scrolling through 16 sets of signals or "monitoring modes". The reset/mode button has a dual function, when pressed for more than two seconds it resets the board, otherwise it is used to scroll through the monitoring modes selecting which set of signals is to be displayed on the 16 LEDs. When the monitoring mode is changed, only one of the front panel LEDs is briefly turned on to show the active mode number. Each bi-color LED is actually made by a red and a green LED in the same package. The red LED is driven by the signal to be monitored and the green LED by the same signal negated, both of them are stretched to have a minimum duration of 150msec in order to be visible to the human eye. The front panel accessible diagnostic uses minimal space/resources, does not require any external interface to check a large number of signals and flags and has proven to be extremely useful during system testing and commissioning.

## VI. MIXER SYSTEM CONFIGURATION

One of the 17 FPGAs on each mixer board acts as the board controller and is automatically configured at power-up by an on-board EEPROM. The EEPROM contents are modifiable through a front panel JTAG (IEEE Std 1149.1) interface port. The board controller interacts with the subrack controller and handles the configuration of the remaining 16 FPGAs. The FPGAs configuration files are stored on a removable CompactFlash card [17] on the subrack controller. At power-up the configuration time for the full mixer system is 30 seconds.

## VII. TESTING THE MIXER SYSTEM

Mixer system testing has been a fundamental step necessary to solve assembly problems, verify system performance, timing and guarantee error free operation. The testing went through three phases.

### A. Intra-board connectivity

The first phase of testing was a connectivity test that verified the trace and solder connections between all of the FPGAs and their auxiliary logic. This portion of the test was done using Corelis™ [18] boundary scan software that allows the user to access and test the I/O interconnects on any JTAG capable device.

### B. Data transfer accuracy

The second phase of testing involved verification of the data paths, the reorganization algorithms, and timing. Because the Mixer system is logically partitionable into five independent and identical subsystems, a subsystem of four adjacent Mixer boards were used for this phase of testing.

A custom test-board called the *Datapump* [6] was used to exercise the mixer subsystem input links with test patterns and

analyze the mixer subsystem output links. The Datapump test-board was connected to a host computer's parallel port and controlled by a user interface based on MS Excel™ [19]. This test system allowed comparing the data transmitted on the mixer subsystem output links with the software-generated expected data and to verify mixer board diagnostic functionality.

### C. In-situ testing

Final testing was done during commissioning at the D0 experiment site in the Mixer System subrack installed on the D0 detector platform. Tests included verification of input/output links cabling using the mixer test pattern detection/transmission capability and frame timing/synchronization using the mixer system diagnostic.

## VIII. CONCLUSION

The Mixer system was installed in November of 2001. The system has proven reliable and accurate. The mixer system diagnostic has played an important role in solving issues during Central Fiber Tracker electronics integration and is currently used by the D0 experiment online software to continuously monitor CFT system performance.



Fig. 4. The Mixer subrack showing the custom backplane, three Mixer boards, and a subrack controller installed. The digital multi-meter is shown for size reference.

## IX. ACKNOWLEDGMENT

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